501.32049RV1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yujiro KAJIHARA *et al.*

Serial No.: Unassigned (Rule 53b Divisional of 09/328,910)

Filed: 16 November 2001

For: LEAD FRAME SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, USING THE SAME, AND METHOD OF AND PROCESS FOR FABRICATING THE TWO

Art Unit: Unassigned (Parent - 2815)

Examiner: Unassigned (Parent - J. Clark)

PRELIMINARY AMENDMENT

Honorable Commissioner for Patents
Washington, D.C. 20231

16 November 2001

Sir:

Prior to calculating the filing fee for the above-identified divisional reissue application, entry of the following amendments is respectfully requested.

IN THE SPECIFICATION:

Please replace the paragraph at Column 1, lines 5-7 with the following amended paragraph:

--Notice: More than one reissue application has been filed for the reissue of U.S. Patent No. 5,637,913. The reissue applications are Serial No. 09/328,910 filed 9 June 1999, pending, and its divisional applications, Serial No. _____ filed 16 November 2001 (the present application), pending, and Serial No. _____ filed 19 November 2001, pending.--

Please replace the paragraph at Page 3, Column 6, lines 31-41 with the following amended paragraph:

--In case the aforementioned individual portions are formed by the pressing, burrs 11 are left on the back of the cut portions. Since the leadframe 1 of the present embodiment is made such that the die pad 3 has a smaller area than that of the semiconductor chip 2 to be mounted thereon, the burrs 11, if any, on the face of the die pad 3 for mounting the semiconductor chip 2 will be unable to mount the chip 2. When the die pad 3 is to be pressed, therefore, it is pressed with its chip mounting [Face] face being directed upward so that the burrs 11 may be left on the back opposed to the chip mounting face.--.

Please replace the paragraph at Page 4, Column 8, lines 46-50 with the following amended paragraph:

--As shown in FIG. 15, moreover, slightly wider small pads (or adhesion-applied portions) 20 than the suspension leads 4 may be formed around he die pad 5 so that the adhesive [1S] 15 may be applied to the individual principal faces of the die pad 3 and the small pads 20.--.

IN THE CLAIMS:

Please cancel Claims 37-49, without prejudice or disclaimer.

Please add new Claims 15-27, as follows.

15.(New) A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof;

(b) a lead frame having:

a chip mounting portion having one surface for mounting said semiconductor chip; and

a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion and being arranged at a periphery of said chip mounting portion, said inner lead portions of said plurality of leads being electrically connected with said bonding pads of said semiconductor chip; and

(c) a resin member sealing said semiconductor chip, said chip mounting portion and said inner lead portions of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip, and

wherein said one surface of said chip mounting portion is a surface on which burrs are not formed, during formation of said chip mounting portion.

16.(New) A semiconductor device according to Claim 15, wherein said burrs are formed when said lead frame is made by pressing.

17.(New) A method of manufacturing a semiconductor device according to Claim 15, wherein said chip mounting portion has a substantially circular form in a plane view.

18.(New) A method of manufacturing a semiconductor device according to Claim 16, wherein said chip mounting portion has a substantially cross form in a plane view.

19.(New) A semiconductor device according to Claim 15, wherein said inner lead portions of said plurality of leads are electrically connected with said bonding pads of said semiconductor chip by a plurality of bonding wires.

20.(New) A semiconductor device according to Claim 19, wherein parts of said inner lead portions of said plurality of leads, to which said plurality of bonding wires are connected, are plated.

21.(New) A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof;

(b) a lead frame having:

a chip mounting portion for mounting said semiconductor chip; and

a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion and being arranged at a periphery of said chip mounting portion,

(c) a plurality of bonding wires electrically connecting said inner lead portions of said plurality of leads with said bonding pads of said semiconductor chip respectively, each of said inner lead portions of said plurality of leads having one surface to which a corresponding bonding wire among said plurality of bonding wires is connected; and

(d) a resin member sealing said semiconductor chip, said plurality of bonding wires, said chip mounting portion and said inner lead portions of said plurality of leads,

wherein said one surface of said inner lead portion of each of said plurality of leads is a surface on which burrs are formed, said burrs being resultant from formation of said plurality of leads.

22.(New) A semiconductor device according to Claim 21, wherein a size of said chip mounting portion is smaller than that of said semiconductor chip.

23.(New) A semiconductor device according to Claim 21, wherein said burrs are formed when said lead frame is made by pressing.

24.(New) A semiconductor device according to Claim 22, wherein said chip mounting portion has a substantially circular form in a plane view.

25.(New) A semiconductor device according to Claim 22, wherein said chip mounting portion has a substantially cross form in a plane view.

26.(New) A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof;

(b) a lead frame having:

a chip mounting portion having a first surface for mounting said semiconductor chip; and

a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion and being arranged at a periphery of said chip mounting portion;

(c) a plurality of bonding wires electrically connecting said inner lead portions of said plurality of leads with said bonding pads of said semiconductor chip respectively, each of said inner lead portions of said plurality of leads having a second surface to which a corresponding bonding wire among said plurality of bonding wires is connected; and

(d) a resin member sealing said semiconductor chip, said plurality of bonding wires, said chip mounting portion and said inner lead portions of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip,

wherein said first surface of said chip mounting portion is a surface on which burrs are not formed, and

wherein said second surface of said inner lead portion of each of said plurality of leads is a surface on which said burrs are formed, said burrs resultant from formation of said chip mounting portion and said plurality of leads.

27.(New) A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof;

(b) preparing a lead frame having:

a chip mounting portion having one surface for mounting said semiconductor chip, a size of said chip mounting portion being smaller than that of said semiconductor chip; and

a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion and being arranged at the periphery of said chip mounting portion, wherein said one surface of said chip mounting portion is a surface on which burrs are not formed, said burrs resultant from formation of said chip mounting portion by pressing;

(c) after the step (b), mounting said semiconductor chip on said one surface of chip mounting portion;

(d) electrically connecting said inner lead portions of said plurality of leads with said bonding wires of said semiconductor chip by a plurality of bonding wires respectively; and

(e) sealing said semiconductor chip, said plurality of bonding wires, said chip mounting portion and said inner lead portions of said plurality of leads.

REMARKS

This Preliminary Amendment submits the following amendments and remarks for entry and consideration in the present divisional reissue application.

STATUS OF CLAIMS AND SUPPORT FOR CLAIM CHANGES

Claims 1-14 were issued in the original patent upon which the parent reissue application of the present divisional reissue case is based. Unrelated to any prior art rejection, Claims 1-14 have been deleted herein, and new Claims 15-27 are submitted herein. New Claims 15-27 are substantially identical to Claims 37-49, which were cancelled without prejudice or disclaimer in the parent reissue application of the present divisional reissue case, and find full support in the patent as issued and the parent reissue application. No new matter is added.

Applicant respectfully notifies the Office that further amendments to the claims may be made in one or more subsequently-filed Preliminary Amendments in order to adjust a clarity and focus of Applicant's claimed invention and to correct the error upon which the parent reissue and the present divisional reissue cases are based.

At entry of this paper, Claims 15-27 are pending in the application for consideration and examination.

DISCLOSURE/SPECIFICATION AMENDMENTS

In the parent reissue application of the present divisional reissue case, the disclosure/specification was objected because of minor informalities. Therefore, the amendments to the specification that have been adopted in the parent reissue application are repeated in the present divisional reissue case.

Further, the specification has been amended to comply with the necessary Notice indicating more than one application filed for reissue of a single patent, and such Notice will be updated upon receipt of the required information by Applicant.

Any spelling, idiomatic, grammatical and/or other informality noted during any further review of the disclosure/specification will be corrected.

NON-REWRITTEN ALLOWABLE CLAIMS

Although Claims 39, 40, 46 and 47 were indicated as being allowable if rewritten as indicated at Section 4 on page 5 of the Office Action mailed 11 June 2001 in the parent reissue application of the present divisional reissue case, rewriting has not been effected. Applicant respectfully reserves the right to amend the potentially allowable claims at a later time if necessary, and Applicant and the undersigned respectfully thank the Examiner for such indication of potentially allowable subject matter.

REJECTIONS UNDER 35 USC § 103 - TRAVERSED

All prior art rejections of Claims 15-27 (previously Claims 37-49) made in the parent reissue application of the present divisional reissue case (*i.e.*, the 35 USC §103 rejection of Claims 37, 38, 41, 43-45, 48 and 49 as being unpatentable over Mori *et al.* (U.S. Patent 4,857,989) in view of Umeda (JP 1-216563) and Kohara *et al.* (U.S. Patent 4,937,656); and the 35 USC §103 rejection of Claim 42 as being unpatentable over Mori *et al.* in view of Umeda and Kohara *et al.*, and further in view of Kanzaki *et al.* (U.S. Patent 5,205,878)) are respectfully traversed herein.

Further, all descriptions of Applicant's disclosed and claimed invention, and all descriptions and rebuttal arguments regarding the applied prior art, as previously submitted by Applicant in any form, are repeated and incorporated herein by

reference. Moreover, all Office Action statements regarding the prior art rejections are respectfully traversed.

Therefore, Applicant respectfully requests reconsideration and withdrawal of such rejections.

CLAIM FOR PRIORITY

Applicant hereby claims priority under 35 USC §119 of JP 4-320098 filed 30 November 1992 and JP 4-71116 filed 27 March 1992. The certified copies of the priority documents were submitted on 29 March 1993 in prior application Serial No. 08/038,684, which matured into U.S. Patent No. 5,637,913, the patent on which the parent reissue and the present divisional reissue cases are based. Acknowledgment of the claim for priority in this divisional reissue application is courteously solicited.

INFORMATION DISCLOSURE STATEMENT

Attached hereto are Forms PTO-1449 listing all of the references cited to or by the Office in the patented file and the parent reissue application upon which this divisional reissue application is based. In accordance with 37 CFR §§ 1.97 and 1.98, Applicant respectfully requests entry and consideration of the information listed on the attached Forms PTO-1449 so that they appear on the printed face of any reissue patent issuing on the present divisional reissue application.

EXAMINER INVITED TO TELEPHONE

The Examiner is herein invited to telephone the undersigned attorneys at the local Washington, D.C. area telephone number of 703-312-6600 for discussing any

Examiner's Amendments or other suggested actions for accelerating prosecution and moving the present application to allowance.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that the claims listed above as presently being under consideration in this divisional reissue application are now in condition for allowance. Accordingly, early allowance of such claims is respectfully requested.

Please charge any shortage in fees necessitated by this Preliminary Amendment or divisional reissue application, including excess claim fees, to ATS&K Deposit Account No. 01-2135 (as Order No. 501.32049RV1), and credit any overpayment or excess fee thereto.

Respectfully submitted,

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ATTACHMENTS:
APPENDIX A-MARKED VERSION
Forms PTO-2038 (2)

APPENDIX A-MARKED VERSION

Paragraph at page 6, lines 31-41:

In case the aforementioned individual portions are formed by the pressing, burrs 11 are left on the back of the cut portions. Since the leadframe 1 of the present embodiment is made such that the die pad 3 has a smaller area than that of the semiconductor chip 2 to be mounted thereon, the burrs 11, if any, on the face of the die pad 3 for mounting the semiconductor chip 2 will be unable to mount the chip 2. When the die pad 3 is to be pressed, therefore, it is pressed with its chip mounting [Face] face being directed upward so that the burrs 11 may be left on the back opposed to the chip mounting face.

Paragraph at page 8, lines 46-50:

As shown in FIG. 15, moreover, slightly wider small pads (or adhesion-applied portions) 20 than the suspension leads 4 may be formed around he die pad 5 so that the adhesive [1S] 15 may be applied to the individual principal faces of the die pad 3 and the small pads 20.